REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

In the office action (page 2), claim 5 has been rejected under 35 U.S.C. 112, ¶2 on grounds that the limitation "the at least one state signal" in line lack sufficient antecedent basis.

In response, "the" has been removed. Withdrawal of the rejection is respectfully requested.

In the office action (page 3), claims 1-3, 5, and 21 have been rejected under 35 U.S.C. 103(a) as being obvious over U.S. Publication No. 2003/0117356 (Moon) in view of U.S. Patent No. 5,764,212 (Nishitani).

The applicants **disagree**. The applicants have amended claim 1 to incorporate all limitations of claim 2 (now cancelled) and respectfully submit that the amended claim 1 is not taught or suggested by Moon or Nishitani, whether these references are considered individually or in combination.

The structure(s) and method(s) as disclosed in Moon or Nishitani are quite different from the presently claimed invention.

For starters, the examiner is respectfully referred to the FIGS. 1-3 (Prior Art) of the present application, were the first, second, and third gate off voltages VG01, VG02, VG03 as shown in FIG. 3 (Prior Art) are offsetted due to the resistances R1, R2, etc. as shown in FIG. 1 that are found in the signal line pattern 22 as shown in FIG. 2 (Prior Art). The resulting voltage drops and signal delays caused by the signal line pattern 22 causes "variance in charge quantity and leakage quantify of data voltage" and as a result "it causes a screen quality problem, such as a block phenomenon showing that blocks of a gate driver ICs display different brightness from each other, variation of uniformity and flicker between an upper end and a lower end of a screen, and degradation of response speed" (specification page 5, lines 10-24).

The Background section on page 6 discusses three prior art attempts to solve these problems, one of which of particularly noted:

"Still another method is to coincide a **resistance value** of an inside signal line

> patterns existed in the gate driver ICs 20 with that of the signal line patterns of the panel so that non-uniformity of a screen caused at boundary faces among the gate driver ICs 20 is reduced. However, this method has an economic problem in that design of the gate driver ICs must be changed every time according to several variables, such as size and resolution of a liquid crystal panel, etc." (specification page 6, line 19 to page 7, line 3)

The cited Moon reference is quite unlike the presently claimed invention, but is quite the same as the above mentioned prior art solution as described in the specification page 6, line 19 to page 7, line 3.

Moon [0005] at page 4 specifically teaches use of a "compensating resistor" as follows:

> "[0055] In order to compensate for voltage differences in gate driving signal is applied to each gate driver ICs 48A to 48D generated by an intrinsic line resistance within the first to fourth LOG gate low voltage transmission lines VGLL1 to VGLL4, **compensating resistor** may be included within each of the gate driver IC's 48A to 48D" (Moon [0055]).

Moon FIGS. 4A-4D and [0056] at page 4 clearly shows this where the different "compensating resistors" are provided at the gate voltage terminals of each of the first to the fourth gate driver ICs 48A to 48D. For this reason, the structure as disclosed in Moon utilizing resistors (see FIGS. 4A-4D) at each gate drive ICs (see FIG. 3, 48A, 48B, 48C, 48D) to compensate for the voltage drop across each gate drive ICs 48A, 48B, 48C, 48D. Thus, the structure of Moon would still bear all of the "economic problems" of the prior art mentioned in the Background section of the present disclosure (page 6, line 23 to page 7, line 3), at least since the design of the gate driver ICs 48A, 48B, 48C, 48D must be changed every time for different LCDs according to several variables, such as size and resolution of a liquid crystal panel, etc.

With this understanding of Moon in mind, the examiner is respectfully pointed out that the office action page 3 incorrectly characterizes the Moon's invention. This is because Moon relating to the prior art method of utilizing the "compensating resistors" **cannot** teach the claimed --sequence recognition unit-- (such as FIGS. 8-9, 60, 60a, 60b) that is the novel design to cure the deficiencies of the prior art designs such as the Moon's "compensating resistors."

The examiner, without providing a specific support in Moon in the office action page 3, incorrectly alleges that the claimed --sequence recognition unit-- is merely a "means included in one of 'gate TCPs 46A-46D,' receiving one of 'gate start pulse' and 'gate enable signal' [fig. 2 and par. (0054) lines 1-9]" in the office action page 3.

Moon's TCPs 46A-46D are merely the TCPs (i.e., taped carrier packages) housing the gate driver ICs 48A-48D (see Moon [0055]-[0056] at page 4), and this structure of Moon is no different than the FIG. 1 (Prior Art) TCP 18 housing a gate driver IC 20 in the Background of the present application. Accordingly, Moon's TCPs 46A-46D having the gate driver ICs 48A-48D operate in the same manner as the FIGS. 1-2 (Prior Art) of the present application to supply gate driving signal to gate lines (such as G_L) albeit with **one difference** that each of Moon's TCPs 46A-46D utilizes a "compensating resistor" to take care of the problem related to inherent voltage drop of the signal line pattern across each of the TCPs. As Moon specifically teaches using "compensating resistor" to each TCP 46A-46D to address this problem of voltage drop in the signal line pattern due to its inherent resistance, Moon's TCP 46A-46D does **not** require or include the following sequence recognition limitation in each of TCPs 46A-46D recited in claim 1 as follows:

> --**a sequence recognition unit** for recognizing sequence of a pertinent gate driver IC from a plurality of gate driver ICs by a pulse width of a vertical start signal inputted in synchronization with a vertical synchronous signal, and generating a carry signal and location data of the pertinent gate driver IC--.

The examiner in the office action page that the claimed --sequence recognition unit-- is merely a "means included in one of 'gate TCPs 46A-46D' [of Moon]" is based on an impermissible hindsight reasoning. The basis for improperly finding the presently claimed invention as though the "sequence recognition unit" could be found in Moon's TCPs 46A-46D is based on the teachings found in this application, and not in the prior art. Thus, the rejection in the Office Action page 3 over Moon improperly relies on the **impermissible hindsight reasoning**, because the rejection would not stand absent the applicants' disclosure in this application that discloses the claimed --sequence recognition unit-- that is provided to the gate driver ICs to solve the particular problems inherent to the prior art such as Moon utilizing compensating resistors. (See 37 C.F.R.

§ 1.104(c)(2).)

According to MPEP §2142, the hindsight reasoning based on the applicant's own disclosure is not permitted. Knowledge of the applicants' disclosure must be set aside. The examiner must step back in time to when the invention was unknown and just before it was made. Only the fact gleaned from the prior art may be used.

When the examiner is still not persuaded by this, the examiner is invited to specifically point out where in the Moon's TCPs 46A-46D is taught the claimed --sequence recognition unit--. Otherwise, withdrawal of the rejection is proper and is respectfully requested.

Moving on to the office action page 4, the applicants agree and the examiner is correct to the extent that "Moon does not expressly teach the sequence recognizing sequence of gate driver IC ...," and this is because nowhere in Moon makes use of or requires the claimed --sequence recognition unit-- for the same reasons as asserted above. Then neither Moon nor Nishitani can suggest the requisite desirability for combination (MPEP §2143.01). The mere fact that Nishtani teaches a counter that, however, is applied in a totally different design for a totally different purpose than the presently claimed invention does **not** provide sufficient rationale that the counter of Nishtani **can** be modified or combined with Moon, which does not even teach the claimed --sequence recognition unit--. Further, when not every limitation recited in claim 1 is taught by Moon as asserted above and admitted by the examiner, there is no prima facie case of obviousness. Neither Moon nor Nishtani provides a sufficient motivation or suggestion to combine and make the resultant combination prima facie obvious.

For the reasons above, the examiner is respectfully requested to withdraw the rejection and provide indication of allowable subject matter.

In the office action (page 7), claims 13-20 are allowed.

The applicants thank the examiner.

For the reasons set forth above, the applicants respectfully submit that claims 1, 3, 5, and 13-22, now pending in this application, are in condition for allowance, if they

are not already allowed. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

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